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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,337	04/21/2004	Takashi Yamada	251383US2CONT	5457
22850	7590	09/09/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			SOWARD, IDA M	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	

2822

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/828,337

**Applicant(s)**

YAMADA ET AL.

**Examiner**

Ida M. Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 29-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 35-48 is/are allowed.
- 6) ☒ Claim(s) 29-31 is/are rejected.
- 7) ☒ Claim(s) 32-34 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 09/995,594.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/21/04 &amp; 1/31/05</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office Action is in response to the preliminary amendment filed April 21, 2004.

#### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/995,594, filed on 11/29/2001.

#### ***Information Disclosure Statement***

The information disclosure statement filed 04/21/2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because there are no copies of the Foreign Patent Documents and the Non Patent Literature Documents listed. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

#### ***Specification***

The abstract of the disclosure is objected to because "**comprises**" should have been **includes** on line 3, page 41. Correction is required. See MPEP § 608.01(b).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanigawa (5,740,099).

In regard to claim 29, Tanigawa teaches a semiconductor chip comprising: a base substrate 30e; a bulk device region 30b having a bulk growth layer 30f & 30g on a part of the base substrate 30e, the bulk device region 30b having a first device-fabrication surface in which a bulk device Qn1 & Qp1 is positioned on the bulk growth layer 30f & 30g; a pn junction formed in the bulk device region 30b and positioned above an interface between the base substrate 30e and the bulk growth layer 30f & 30g; an SOI device region 30a having a buried insulator 30c on the other part of the base substrate 30e and an SOI layer on the buried insulator 30c, the SOI device region 30a having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; a first isolation 30 formed in the bulk device region 30b so as to separate the bulk device Qn1 & Qp1, and a second isolation 34 in the SOI device

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region 30a so as to separate the SOI device, the first and second isolations 34 being substantially the same depth and having a depth reaching the buried insulator 30c; and a boundary layer located at a boundary between the bulk device region 30b and the SOI device region 30a (Figure 4, columns 6-8, lines 7-67, 1-67 and 1-12, respectively).

In regard to claim 30, Tanigawa teaches the bulk growth layer 30f & 30g is a silicon bulk growth layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors (column 9, lines 9-15).

In regard to claim 31, Tanigawa teaches a third isolation 34 positioned at the boundary and functioning at the boundary layer, wherein the first, second, and third isolations 34 are of substantially the same depth (Figure 4).

#### ***Allowable Subject Matter***

Claims 35-48 are allowed.

Claims 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent

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claims, such as a dummy trench formed in the bulk device region between the bulk device and the SOI device. The dependent claims being further limiting and definite are also allowable.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor chip structures:

Christensen et al. (US 6,528,853 B2)	Leobandung et al. (US 6,429,488 B2)
Pearce (5,777,362)	Tada (5,973,366).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

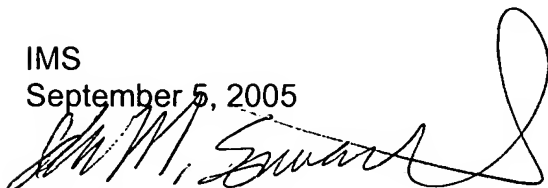
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS

September 5, 2005

  
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